UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/475,614	12/30/1999	Gilbert Wolrich	10559/137001/P7876	6580

20985 7590 09/16/2005

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
ENG, DAVID Y	
ART UNIT	**PAPER NUMBER**
2155	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/475,614
Filing Date: December 30, 1999
Appellant(s): WOLRICH ET AL.

Robert A. Greenberg
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 25, 2005 appealing from the Office action mailed January 19, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

09/626,535 filed 7/27/2000

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

Claims 1-24 and 44 stand rejected under 35 USC 103(a) over Allison (USP 6,373,848) in view of Belkin (USP 6,604,125).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,604,125 Belkin 8-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-24 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allison (USP 6,373,848) in view of Belkin (USP 6,604,125).

Appellants provide separate arguments for independent claims 1, 17 and 18 but not dependent claims 2-16, 19-24 and 44. Dependent claims 2-16 and 44 therefore stand or fall with their parent independent claim 1 and dependent claims 19-24 stand or fall with their parent independent claim 18. Independent claim 17 has no dependent claim.

Independent claims 1 and 18 are one step method claims. Independent claim 17 is most comprehensive among claims 1, 17 and 18 and includes all the limitations of claims 1 and 18. Claim 17 therefore is selected as an exemplary in the art rejection.

Teaching of Allison

Allison teaches a multi-port MAC (Media Access Control lines 31-33 of column 2). Figure 1 shows that the MAC comprises a plurality of ports for communicating with telephone, fax machine and modem, etc. (column 1, lines 20-22), a pair of FIFO registers 40 and 43 for transceiving data to/from the network (see "network" in lines 39 and 42 of column 2) via connected ports and a multiplexer for selecting one of the ports from a plurality of ports. Figure 1 further shows that the MAC is connected to a host.

Figure 9 depicts a flow chart for showing operation of data transfer between selected one of the ports and the host via the MAC.

Rejection of the claims

Appellants' invention is for transferring data from one of a plurality of ports to a memory.

With respect to claim 17, reference is made to the abstract, Figures 1 and 9 and the description thereof in Allison. Allison teaches:

a method (column 2, line 43) of receiving data from a plurality of peripheral ports (port 0 to port N, Figure 1), comprising:

determining that the one of the plurality of peripheral ports requires servicing (inherent in a system having multiple ports; see port selector 46 in Figure 1; see also Figure 9 step 100);

issuing a receive request based on the determination, the receive request (inherent in a port selector) directing the transfer of data from the one of the plurality of peripheral ports to a buffer memory (Figure 1 shows that port selector 46 together with multiplexer 18 select one port from a plurality of N ports for transferring data from the selected port to RX FIFO 43 and further to host 12; see also Figure 9 and the description thereof in column 11) and specifying a program thread (instructions, see line 57, column 2; see also "word entry" in line 63 of column 2 in Allison) from among of a plurality of processing program threads to process (to be processed by control logic 34) the data; and

transferring the data to the buffer memory (transferring data from the selected one of N ports to RxFIFO) and signaling to the specified thread that the data is ready for processing (by control logic 34 of Allison).

Obviousness: Allison uses the term "word" instead of "thread"

Figure 2 of Allison shows that RxFIFO 43 is coupled to RxMAC 28 and RxState Regs & Mux 30. Allison teaches that RxFIFO 43 provides instructions (column 2, lines 57-59) to control logic 34 for controlling transmitting and receiving data between the host system and the network. In lines 62-67 of column 2, Allison further teaches that receive state machine (RxState Regs & Mux 30) contains a state table having one word entry for each port. As the ports are selected by the port selector, the associated word for a port is read from the table and used to control the state machine in servicing the selected port and associated instructions are provided from the RxFIFO 30 to control logic 34. It can be seen that Allison meets the claim limitation of "specifying a thread from among a plurality of processing program threads to process the data" except that Allison uses the terms "word" and "instructions" instead of "program threads" as used by Appellants in describing selected control information for controlling data transfer between a network and a host. Figure 1 of Belkin shows a server 106 for controlling information transfer between clients (computers) via a network 104. The server has a storage for storing a pool of threads and a thread selector. In response to a request, a specific thread from a plurality of threads is selected to process the task (Figure 4). It can be seen that Belkin uses the terms "program threads" in describing selecting a thread form a plurality of program threads. In Allison, the term "word" is used instead of

"thread" because it is a single instruction thread. If Allison requires more than one word in controlling the selected port, it would have been obvious, from the teaching of Belkin, to a person of ordinary skill in the art to use the term "thread" in describing the control information for controlling data transfer between the host and a selected port.

(10) Response to Argument

(1) Allison, pages 6-9 of the Brief

Appellant contended that Allison does not make any mention of executable instructions, program counters or subroutines. Appellants are referring to the applying of the Allison patent in the Office actions to the claim limitation "—specifying a thread from among a plurality of processing program threads to process the data". The claims did not use the terms executable instructions, program counters or subroutines. In the rejection above, the Examiner explains how the combined teaching of Allison and Belkin meet the claim limitations. Appellants' arguments directed to executable instructions, program counters or subroutines are therefore considered moot although it can be said that program counter is inherent in instruction execution and subroutine is an alternate label for program thread. As to the claim limitation of "issuing a request directing a transfer of data from one of a plurality of device ports to a storage unit", the mere fact that the MAC of Allison is for transferring data from one of the ports to a host system is sufficient to meet the claim limitation. Appellants do not disagree that the MAC of Allison is for transferring data from one of the ports to a host system. Figure 9 of Allison clearly shows a flow chart showing how that is done. The initiation of the execution of the instructions or subroutine representing the flow chart of Figure 9 is nothing but a request

to transfer data from one of the ports to a host system. Appellants fail to provide any arguments as to how their request as claimed is patentable distinct from the Allison's request.

(2) Allison in view of Belkin (pages 9-11)

Appellants contended that Allison provides no support for the assertion that the control logic 34 executes thread instructions issued by the RxFIFO 43. The Examiner disagrees. Allison, in lines 57-59 of column 2, clearly discloses how FIFO (RxFIFO and TxFIFO) transfer instructions to control logic for execution. As to using the term "thread", the Examiner relies on Belkin for that teaching.

Appellants further disagree on the Examiner's motivation to combine Allison and Belkin. Firstly, Allison and Belkin are of analogous art. Secondly, the Examiner does not rely on Belkin to technically modify Allison. Rather, the Examiner relies on Belkin for using the term "thread" to describe the term "word" in Allison. Program threads are a collection of groups of instructions each of which has a specific function. A collection of words in Allison is like a collection of threads in Belkin. The term "word" in Allison and the term "thread" in Belkin therefore can be used interchangeably.

(11) Conclusion

Appellants' invention is purported to transfer data from one of the ports to a memory. That is exactly what Allison's MAC chip (Figure 1) is for. The step of determining, issuing, transferring and signaling are inherent in a MAC chip. The only remaining issue is whether Allison teaches specifying a program thread from among of a plurality of processing program threads to process the data. As explained in the

Answer above, Allison teaches a state table having entries for storing control words each of which corresponds to a port. When a port is selected for servicing, the correspondent word is specified to control the transferring of data from that port to a memory. Corresponding instructions are also specified and transferred from the RxFIFO to control logic 34 for execution. It is obvious to use the term "thread" as taught by Belkin to describe the term "word" in Allison. Appellants fail to suggest one single claim limitation, let alone patentable distinct, that is not taught by the applied references. For the reasons set forth above, it is believed that the rejection remains intact. It is therefore respectfully requested that the rejection be sustained.

Respectfully submitted,

David Y. Eng

DAVID Y. ENG
PRIMARY EXAMINER

Conferees:

Saleh Najjah

Zarni Maung

ZARNI MAUNG
SUPERVISORY PATENT EXAMINER

SALEH NAJJAR
PRIMARY EXAMINER